AMENDMENTS TO THE SPECIFICATION:

On page 8 of the Substitute Specification, please amend the paragraph beginning on line 10 and ending on line 24 to read as follows:

Alternatively, the ~~pumps~~ bumps can also be generated on the solderable metallizations on the surface of the chip. This can, for example, likewise ensue via galvanic deposition over the corresponding metallizations. A stencil printing of solder depots on the metallizations and a subsequently remelting process is also possible. Since here the wetting capability of the solderable metallizations also makes the structuring easier, a different wetting capability of metallic structures can also be used for structuring of the bumps on the wafer or, respectively, on the chip. For example, it is possible to passivate the greater part of the metallizations located on the chip, for example via generation of an anodic oxide layer that can additionally be covered with an applied mineral layer, for example a thin silicon oxide layer or a thin silicon nitride layer. The surfaces not covered by this passivation then remain wettable with solder or are specifically made wettable via suitable further layers, what are known as under-bump metallizations – UBM – with solder, while the passivated surfaces of the metallization constitute the solder stop mask.

On page 13 of the Substitute Specification, please amend the paragraph beginning on line 2 and ending on line 7 to read as follows:

Figure 1 shows a first embodiment of an inventive component in schematic cross-section. The component is essentially formed of the chip CH, for example a piezoelectric substrate on whose one surface are applied component structures BS such as, for example, band-shaped metallizations of a surface wave component (SAW component) and which have a height h3. The chip is applied on a carrier substrate TS which comprises at least one upper layer OS and one lower layer US.

On page 13 of the Substitute Specification, please amend the paragraph beginning on line 8 and ending on line 22 to read as follows:

Recesses AN, which have a depth h1, are provided in the upper layer OS of the carrier substrate TS. On the floor of the recesses, solderable connection areas LA are arranged over which the bump connections BU, which have a height h4, are arranged. The

bumps BU connect the solderable connection areas LA with the solderable metallizations LM on the surface of the chip CH. The chip rests on a frame RA which defines the distance between the upper surface of the upper layer OS and the surface of the chip CH and prevents a direct contact of the component structures BS with the carrier substrate TS. In the direct contact with the lower chip edge and the adjacent surface areas of the carrier substrate, the entire chip is arranged surrounded by a solder border LR that seals the chip CH to the carrier substrate TS. Between upper layer OS and lower layer US, conductor traces LB are provided that can form a wiring plane. Further feedthroughs DK through the lower layer US or, as the case may be, further layers achieve an electrically-conductive connection to the electrical connections for the contacting of the component outwards, for example to the SMD-capable contacts KO on the underside of the carrier substrate.